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<b>FEE TRANSMITTAL</b>		U.S. Department of Commerce Patent and Trademark Office		<b>COMPLETE IF KNOWN</b>																																																			
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		First Named Inventor		Ji-Young LEE																																																			
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METHOD OF PAYMENT (check one)																																																							
1. <input type="checkbox"/> The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:  Account Number: <b>02-4943</b> Deposit Account Name:  <input checked="" type="checkbox"/> Charge any additional fee required under 37 CFR 1.16 and 1.17  <input type="checkbox"/> Charge the issue Fee set in 37 CFR 1.18 at the mailing of the Notice of Allowance. 37 CFR 1.311 (b).			2. <input checked="" type="checkbox"/> Payment enclosed:  <input checked="" type="checkbox"/> Checks #20693 & #20696  <input type="checkbox"/> Money order  <input type="checkbox"/> Other																																																				
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1. Filing FEE  <table style="width:100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2">Large Entity</th> <th colspan="2">Small Entity</th> <th></th> <th></th> </tr> <tr> <th>Fee Code</th> <th>Fee(s)</th> <th>Fee Code</th> <th>Fee(s)</th> <th>Fee Description</th> <th>Fee Paid</th> </tr> </thead> <tbody> <tr> <td>101</td> <td>770</td> <td>201</td> <td>385</td> <td>Utility filing</td> <td>\$770.00</td> </tr> <tr> <td>106</td> <td>320</td> <td>206</td> <td>160</td> <td>Design filing fee</td> <td></td> </tr> <tr> <td>107</td> <td>530</td> <td>207</td> <td>265</td> <td>Plant filing Fee</td> <td></td> </tr> <tr> <td>106</td> <td>770</td> <td>206</td> <td>385</td> <td>Reissue filing fee</td> <td></td> </tr> <tr> <td colspan="5" style="text-align: right;">SUBTOTAL(1)</td> <td>\$770.00</td> </tr> </tbody> </table>				Large Entity		Small Entity				Fee Code	Fee(s)	Fee Code	Fee(s)	Fee Description	Fee Paid	101	770	201	385	Utility filing	\$770.00	106	320	206	160	Design filing fee		107	530	207	265	Plant filing Fee		106	770	206	385	Reissue filing fee		SUBTOTAL(1)					\$770.00	ADDITIONAL FEES Large Entity  <table style="width:100%; border-collapse: collapse;"> <thead> <tr> <th>Fee Code</th> <th>Fee(s)</th> <th>Fee Description</th> <th>Fee Paid</th> </tr> </thead> <tbody> <tr> <td>581</td> <td>40</td> <td>Assignment Recordation</td> <td>\$40.00</td> </tr> </tbody> </table>		Fee Code	Fee(s)	Fee Description	Fee Paid	581	40	Assignment Recordation	\$40.00
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2. CLAIMS  <div style="text-align: right;">Fee from below</div> Total Claims: <u>23</u> independent claims: <u>2</u> Multiple Dependent claims: _____  <table style="width:100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2">Large Entity</th> <th colspan="2">Small Entity</th> <th></th> <th></th> </tr> <tr> <th>Fee Code</th> <th>Fee(s)</th> <th>Fee Code</th> <th>Fee(s)</th> <th>Fee Description</th> <th>Fee Paid</th> </tr> </thead> <tbody> <tr> <td>102</td> <td>80</td> <td>202</td> <td>40</td> <td>Independent claim in excess of three</td> <td></td> </tr> <tr> <td>103</td> <td>22</td> <td>203</td> <td>11</td> <td>Claim s in excess of 20</td> <td>\$66.00</td> </tr> <tr> <td>104</td> <td>260</td> <td>204</td> <td>130</td> <td>Multiple dependent claims</td> <td></td> </tr> <tr> <td>109</td> <td>80</td> <td>209</td> <td>40</td> <td>Reissue independent claims over original patent</td> <td></td> </tr> <tr> <td>110</td> <td>22</td> <td>210</td> <td>11</td> <td>Reissue claims in excess of 20 and over original patent</td> <td></td> </tr> <tr> <td colspan="5" style="text-align: right;">SUBTOTAL(2)</td> <td>\$66.00</td> </tr> </tbody> </table>				Large Entity		Small Entity				Fee Code	Fee(s)	Fee Code	Fee(s)	Fee Description	Fee Paid	102	80	202	40	Independent claim in excess of three		103	22	203	11	Claim s in excess of 20	\$66.00	104	260	204	130	Multiple dependent claims		109	80	209	40	Reissue independent claims over original patent		110	22	210	11	Reissue claims in excess of 20 and over original patent		SUBTOTAL(2)					\$66.00				
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Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Submitted herewith is the following patent application:

**Inventor: Ji-Young LEE**

**Title: METHOD FOR DETECTING AND SEPARATING VERTICAL  
AND HORIZONTAL SYNCHRONOUS SIGNALS FROM  
COMPUTER SYSTEM**

Please find attached hereto an application for patent which includes: Specification and Abstract, Claims, original Declaration And Power of Attorney, Assignment, and a certified copy of the foreign priority document identified below:

Verified Showing of Small Entity Status: No

Drawings: Formal drawings, 7 sheets, Figures 1 through 7C

Claim of priority under 35 U.S.C. §119: **YES**

**\*\*REPUBLIC OF KOREA** Application No. 96-22949 filed on 21 June 1996

Fee (see formula below): **CHECK IS ENCLOSED**

Basic Fee \$385/770 .....	<b><u>\$770.00</u></b>
Additional Fees:	
Total number of claims in excess of 20 <u>3</u> times \$11/22 .	<b><u>\$66.00</u></b>
Number of independent claims in excess of 3: <u>0</u> times \$40/80 .....	<b><u>\$0.00</u></b>
Multiple Dependent Claims \$130/260 .....	<b><u>\$0.00</u></b>
An Assignment is likewise enclosed: Recording Fee \$40 . .	<b><u>\$40.00</u></b>
Filing Non-English specification .....	<b><u>\$ 0.00</u></b>
<b>TOTAL FEES FOR THE ABOVE APPLICATION .....</b>	<b><u>\$876.00</u></b>

**TITLE**

**METHOD FOR DETECTING AND SEPARATING VERTICAL  
AND HORIZONTAL SYNCHRONOUS SIGNALS  
FROM A COMPUTER SYSTEM**

**CLAIM OF PRIORITY**

This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C §119 from an application entitled *Method For Detecting And Separating Vertical And Horizontal Synchronous Signals From Computer System* earlier filed in the Korean Industrial Property Office on 21 June 1996, and there duly assigned Serial No. 06-22949 by that Office.

**BACKGROUND OF THE INVENTION**

**Field of the Invention**

The present invention relates in general to a monitor which is used as a video display unit of a computer system, and more particularly to a method for detecting and separating vertical and horizontal synchronous signals from the computer system.

**Description of the Prior Art**

Generally, the user monitors and checks the operation status of a computer system by means of a monitor. The computer system outputs a signal based on the current operation and the monitor displays the output signal from the computer system on its screen. The monitor utilizes vertical and horizontal synchronous signals to display the output signal from the computer system on the screen.

1 For this reason, the computer system outputs the vertical and horizontal synchronous signals to the  
2 monitor together with data to be displayed on the screen of the monitor. The computer system  
3 outputs the vertical and horizontal synchronous signals in various manners.

4 For example, the computer system may output the vertical and horizontal synchronous  
5 signals separately or as one composite synchronous signal wherein the vertical and horizontal  
6 synchronous signals are combined. Alternatively, the computer system may combine the vertical  
7 and horizontal synchronous signals on a green color signal and output the resultant one synchronous-  
8 on-green (SOG) signal.

9 The monitor must separate the vertical and horizontal synchronous signals from the computer  
10 system from each other to use them individually.

11 For this reason, the monitor has to check input forms of the vertical and horizontal  
12 synchronous signals from the computer system and separate the vertical and horizontal synchronous  
13 signals from each other in accordance with the checked result.

14 The vertical and horizontal synchronous signals from the computer system may be different  
15 in polarity.

16 For example, the polarities of the separated vertical and horizontal synchronous signals may  
17 be both positive or negative. Alternatively, one of the polarities of the separated vertical and  
18 horizontal synchronous signals may be positive and the other may be negative.

19 In the composite synchronous signal, the vertical and horizontal synchronous signals are the  
20 same in polarity. Namely, the polarities of the vertical and horizontal synchronous signals are both  
21 positive or negative. In the synchronous-on-green signal, the polarities of the vertical and horizontal  
22 synchronous signals are both positive.

23 In this connection, the monitor must use hardware to separate and change the polarities of  
24 the separated vertical and horizontal synchronous signals suitably for the use therein.

1 As a result, the exemplary monitor requires additional hardware design work for the  
2 synchronous signal separator, resulting in increases in manufacturing cost and size of a printed  
3 circuit board. For this reason, the manufactured goods are degraded in competitiveness.

#### 4 SUMMARY OF THE INVENTION

5 Therefore, the present invention has been made in view of the above problems, and it is an  
6 object of the present invention to provide a method for detecting and separating vertical and  
7 horizontal synchronous signals from a computer system using a microcomputer.

8 In accordance with the present invention, the above and other objects can be accomplished  
9 by a provision of a method for detecting and separating vertical and horizontal synchronous signals  
10 from a computer system, comprising the first step of scanning a vertical synchronous signal terminal,  
11 a horizontal/composite synchronous signal terminal and a synchronous-on-green terminal of the  
12 computer system to detect input forms of the vertical and horizontal synchronous signals from the  
13 computer system; and the second step of separating the vertical and horizontal synchronous signals  
14 from each other in accordance with the input forms detected at the first step and adjusting polarities  
15 of the separated vertical and horizontal synchronous signals.

#### 16 BRIEF DESCRIPTION OF THE DRAWINGS

17 The above and other objects, features and advantages of the present invention will be more  
18 clearly understood from the following detailed description taken in conjunction with the  
19 accompanying drawings, in which:

20 Fig. 1 is a block diagram illustrating the construction of an exemplary monitor;

21 Figs. 2A to 2C are waveform diagrams of output signals from a computer system in Fig. 1,  
22 wherein:

1 Fig. 2A shows vertical and horizontal synchronous signals;

2 Fig. 2B shows a composite synchronous signal; and

3 Fig. 2C shows a synchronous-on-green signal;

4 Fig. 3 is a block diagram illustrating the construction of a monitor in accordance with the  
5 principles of the present invention;

6 Fig. 4 is a flowchart schematically illustrating a method for detecting and separating vertical  
7 and horizontal synchronous signals from a computer system in Fig. 3 in accordance with the  
8 principles of the present invention;

9 Figs. 5A to 5D are flowcharts in detail illustrating a synchronous signal detection step in Fig.  
10 4;

11 Fig. 6 is a block diagram illustrating the construction of a microcomputer in Fig. 3 for  
12 performing a synchronous signal separation operation in accordance with the principles of the  
13 present invention; and

14 Figs. 7A to 7C are timing diagrams illustrating the operation of a vertical synchronous signal  
15 detector in Fig. 6.

## 16 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

17 Referring to Fig. 1, there is shown in block form the construction of an exemplary monitor.  
18 In this drawing, reference numeral 1 designates a computer system such as a personal computer.  
19 Computer system 1 outputs red, green and blue color signals at its color signal output terminals R,  
20 G and B. Also, computer system 1 selectively outputs a vertical synchronous signal V at its vertical  
21 synchronous signal terminal VS, a horizontal synchronous signal H or a composite synchronous  
22 signal at its horizontal/composite synchronous signal terminal HCS and a synchronous-on-green  
23 signal at its synchronous-on-green terminal SOG.

1           Reference numeral 2 designates a video signal processor. Video signal processor 2 processes  
2           the red, green and blue color signals from computer system 1 in response to the vertical and  
3           horizontal synchronous signals V and H from computer system 1 and outputs the processed color  
4           signals to a cathode ray tube (CRT) 6.

5           Reference numeral 3 designates a synchronous signal separator. Synchronous signal  
6           separator 3 separates the vertical and horizontal synchronous signals V and H from computer system  
7           1 from each other. Namely, when computer system 1 outputs the vertical and horizontal  
8           synchronous signals V and H as shown in Fig. 2A at its vertical synchronous signal terminal VS and  
9           horizontal/composite synchronous signal terminal HCS, respectively, synchronous signal separator  
10          3 merely adjusts polarities of the vertical and horizontal synchronous signals V and H. On the other  
11          hand, when computer system 1 outputs the composite synchronous signal as shown in Fig. 2B at its  
12          horizontal/composite synchronous signal terminal HCS or the synchronous-on-green signal as shown  
13          in Fig. 2C at its synchronous-on-green terminal SOG, synchronous signal separator 3 separates the  
14          composite synchronous signal or the synchronous-on-green signal into the vertical and horizontal  
15          synchronous signals V and H and adjusts the polarities of the separated vertical and horizontal  
16          synchronous signals V and H.

17          Reference numeral 4 designates a microcomputer. On the basis of frequencies of the vertical  
18          and horizontal synchronous signals V and H separated by synchronous signal separator 3,  
19          microcomputer 4 determines that the present mode is a video signal output mode of computer system  
20          1 and controls the monitor in such a manner that it can be operated in the video signal output mode.  
21          Also, microcomputer 4 outputs the vertical and horizontal synchronous signals V and H separated  
22          by synchronous signal separator 3 to a synchronous signal processor 5.

23          Synchronous signal processor 5 processes the vertical and horizontal synchronous signals  
24          V and H from microcomputer 4 and outputs the processed vertical and horizontal synchronous

1 signals V and H to video signal processor 2. As a result, video signal processor 2 processes the  
2 video signal from computer system 1 synchronously with the vertical and horizontal synchronous  
3 signals V and H from synchronous signal processor 5.

4 Further, synchronous signal processor 5 controls a magnetic field of a deflection coil 7  
5 mounted to CRT 6 so that CRT 6 can display a desired picture in response to an output signal from  
6 video signal processor 2. In other words, synchronous signal processor 5 performs horizontal  
7 position, horizontal size, vertical position, vertical size, side pin cushion, slope, pin balance and  
8 top/bottom corrections with respect to the picture which is displayed by CRT 6.

9 The synchronous signals provided by computer system 1 are classified into the separated  
10 vertical and horizontal synchronous signals V and H, the composite synchronous signal and the  
11 synchronous-on-green signal. The exemplary monitor comprises synchronous signal separator 3 as  
12 hardware means for the separation and polarity adjustment of the synchronous signals from computer  
13 system 1.

14 Referring to Fig. 3, there is shown in block form the construction of a monitor in accordance  
15 with the present invention. In this drawing, reference numeral 10 designates a computer system.  
16 Computer system 10 outputs red, green and blue color signals at its color signal output terminals R,  
17 G and B. Also, computer system 10 selectively outputs a vertical synchronous signal V at its vertical  
18 synchronous signal terminal VS, a horizontal synchronous signal H or a composite synchronous  
19 signal at its horizontal/composite synchronous signal terminal HCS and a synchronous-on-green  
20 signal at its synchronous-on-green terminal SOG.

21 The monitor comprises a video signal processor 20 for processing the red, green and blue  
22 color signals from computer system 10 in response to the vertical and horizontal synchronous signals  
23 V and H from computer system 10, a microcomputer 30 for detecting the vertical and horizontal  
24 synchronous signals V and H from the vertical synchronous signal terminal VS,



1 horizontal/composite synchronous signal terminal HCS and synchronous-on-green terminal SOG  
2 of computer system 10, separating the detected vertical and horizontal synchronous signals V and  
3 H from each other and adjusting polarities of the separated vertical and horizontal synchronous  
4 signals V and H, and a synchronous signal processor 40 for processing the vertical and horizontal  
5 synchronous signals V and H from microcomputer 30 and outputting the processed vertical and  
6 horizontal synchronous signals V and H to video signal processor 20 so that video signal processor  
7 20 can process the video signal from computer system 10 synchronously with the vertical and  
8 horizontal synchronous signals V and H. Further, synchronous signal processor 40 controls a  
9 magnetic field of a deflection coil 50 mounted to a CRT 60. CRT 60 deflects electron beams based  
10 on an output signal from video signal processor 20 according to the magnetic field of deflection coil  
11 50 controlled by synchronous signal processor 40 to display a desired picture.

12 The operation of the monitor with the above-mentioned construction in accordance with the  
13 present invention will hereinafter be described in detail.

14 First, computer system 10 outputs red, green and blue color signals of a desired picture to  
15 be displayed, at its color signal output terminals R, G and B. Also, computer system 10 selectively  
16 outputs the vertical and horizontal synchronous signals V and H at its vertical synchronous signal  
17 terminal VS, horizontal/composite synchronous signal terminal HCS and synchronous-on-green  
18 terminal SOG.

19 Microcomputer 30 scans the vertical synchronous signal terminal VS, horizontal/composite  
20 synchronous signal terminal HCS and synchronous-on-green terminal SOG of computer system 10  
21 to check input forms of the vertical and horizontal synchronous signals V and H.

22 Then, microcomputer 30 separates the vertical and horizontal synchronous signals V and H  
23 from each other in accordance with the checked input forms and adjusts the polarities of the  
24 separated vertical and horizontal synchronous signals V and H.

Also, microcomputer 30 determines the present operation mode according to frequencies of the separated vertical and horizontal synchronous signals V and H and controls the monitor in such a manner that it can be operated in the determined operation mode.

Synchronous signal processor 40 processes the vertical and horizontal synchronous signals V and H from microcomputer 30 and outputs the processed vertical and horizontal synchronous signals V and H to deflection coil 50 to control the electron beam deflection of CRT 60.

Video signal processor 20 processes the red, green and blue color signals from computer system 10 in response to the vertical and horizontal synchronous signals V and H from synchronous signal processor 40 and outputs the processed color signals to CRT 60 to display the desired picture on CRT 60.

Fig. 4 is a flowchart schematically illustrating a method for detecting and separating the vertical and horizontal synchronous signals V and H from computer system 10 in Fig. 3 in accordance with the present invention. First, at step S10, microcomputer 30 scans the vertical synchronous signal terminal VS, horizontal/composite synchronous signal terminal HCS and synchronous-on-green terminal SOG of computer system 10 to detect input forms of the vertical and horizontal synchronous signals V and H. Then, at step S20, microcomputer 30 separates the vertical and horizontal synchronous signals V and H from each other in accordance with the input forms detected at the above step S10 and adjusts the polarities of the separated vertical and horizontal synchronous signals V and H.

Figs. 5A to 5D are flowcharts in detail illustrating the synchronous signal detection step S10 in Fig. 4. First, in Fig. 5A, microcomputer 30 checks at step S100 whether the horizontal synchronous signal H is input from horizontal/composite synchronous signal terminal HCS. If the horizontal synchronous signal H is not input from horizontal/composite synchronous signal terminal HCS at step S100, microcomputer 30 checks at step S210 of step S200 whether the vertical

1 synchronous signal V is input from vertical synchronous signal terminal VS. If the vertical  
2 synchronous signal V is not input from vertical synchronous signal terminal VS at step S210, the  
3 microcomputer 30 checks at step S220 of step S200 whether the vertical and horizontal synchronous  
4 signals V and H are input from synchronous-on-green terminal SOG.

5 On the other hand, when the horizontal synchronous signal H is input from  
6 horizontal/composite synchronous signal terminal HCS at the above step S100, microcomputer 30  
7 checks at step S300 whether the vertical synchronous signal V is input from vertical synchronous  
8 signal terminal VS. If the vertical synchronous signal V is not input from vertical synchronous  
9 signal terminal VS at step S300, microcomputer 30 proceeds to step S400 to check whether the  
10 composite synchronous signal is input from horizontal/composite synchronous signal terminal HCS.

11 When the vertical synchronous signal V is input from vertical synchronous signal terminal  
12 VS at the above step S300, microcomputer 30 checks the polarity of the horizontal synchronous  
13 signal H input from horizontal/composite synchronous signal terminal HCS at step S510 of step  
14 S500. In accordance with the polarity checked at step S510, microcomputer 30 proceeds to step  
15 S520 or S530 to check whether the composite synchronous signal or the separated vertical and  
16 horizontal synchronous signals V and H are input.

17 At the above step S210, microcomputer 30 checks at step S211 whether the vertical  
18 synchronous signal V is input from vertical synchronous signal terminal VS. If the vertical  
19 synchronous signal V is input from vertical synchronous signal terminal VS at step S211,  
20 microcomputer 30 determines at step S212 that only the vertical synchronous signal V is input from  
21 vertical synchronous signal terminal VS with no input of the horizontal synchronous signal H from  
22 horizontal/composite synchronous signal terminal HCS. Then, microcomputer 30 performs  
23 synchronous signal separation step S20.

1 On the other hand, when the vertical synchronous signal V is not input from vertical  
2 synchronous signal terminal VS at the above step S211, microcomputer 30 proceeds to step S220  
3 to check whether the synchronous-on-green signal is input from synchronous-on-green terminal  
4 SOG.

5 At the above step S220, microcomputer 30 checks at step S221 whether the horizontal  
6 synchronous signal H is input from synchronous-on-green terminal SOG. If the horizontal  
7 synchronous signal H is not input from synchronous-on-green terminal SOG at step S221,  
8 microcomputer 30 determines at step S222 that no synchronous signal is input.

9 When the horizontal synchronous signal H is input from synchronous-on-green terminal SOG  
10 at the above step S221, microcomputer 30 checks at step S223 whether the vertical synchronous  
11 signal V is input from synchronous-on-green terminal SOG. If the vertical synchronous signal V  
12 is not input from synchronous-on-green terminal SOG at step S223, microcomputer 30 determines  
13 at step S224 that only the horizontal synchronous signal H is input from synchronous-on-green  
14 terminal SOG with no input of the vertical synchronous signal V. Then, microcomputer 30 performs  
15 synchronous signal separation step S20.

16 However, if the vertical synchronous signal V is input from synchronous-on-green terminal  
17 SOG at the above step S223, microcomputer 30 determines at step S225 that the vertical and  
18 horizontal synchronous signals V and H are together input from synchronous-on-green terminal SOG  
19 and the polarities thereof are both positive. Then, microcomputer 30 performs synchronous signal  
20 separation step S20.

21 At the above step S400 of checking whether the composite synchronous signal is input from  
22 the horizontal/composite synchronous signal terminal HCS, as shown in Fig. 5B, microcomputer 30  
23 checks the polarity of the horizontal synchronous signal H input from horizontal/composite  
24 synchronous signal terminal HCS at step S410. If the polarity checked at the above step S410 is

1 positive, microcomputer 30 performs a first composite synchronous signal detection operation at step  
2 S420. To the contrary, if the polarity checked at the above step S410 is negative, microcomputer  
3 30 performs a second composite synchronous signal detection operation at step S430.

4 At the above step S420 of performing the first composite synchronous signal detection  
5 operation, microcomputer 30 sets the polarity of the horizontal synchronous signal H to positive at  
6 step S421. Also, microcomputer 30 sets the present mode to a vertical synchronous signal extraction  
7 mode. Then, microcomputer 30 checks at step S422 whether the vertical synchronous signal V is  
8 input from horizontal/composite synchronous signal terminal HCS.

9 When the vertical synchronous signal V is input from horizontal/composite synchronous  
10 signal terminal HCS at the above step S422, microcomputer 30 determines at step S423 that the  
11 composite synchronous signal is input from horizontal/composite synchronous signal terminal HCS  
12 and the polarities of the vertical and horizontal synchronous signals V and H are both positive.  
13 Then, microcomputer 30 clamps a back porch of the horizontal synchronous signal H to a reference  
14 level of the picture to be displayed on CRT 60 and performs synchronous signal separation step S20.

15 However, when the vertical synchronous signal V is not input from horizontal/composite  
16 synchronous signal terminal HCS at the above step S422, microcomputer 30 determines at step S424  
17 that only the horizontal synchronous signal H is input from horizontal/composite synchronous signal  
18 terminal HCS. Then, microcomputer 30 clamps a front porch of the horizontal synchronous signal  
19 H to the reference level of the picture to be displayed on CRT 60 and performs synchronous signal  
20 separation step S20.

21 At the above step S430 of performing the second composite synchronous signal detection  
22 operation, microcomputer 30 sets the polarity of the horizontal synchronous signal H to negative at  
23 step S431. Also, microcomputer 30 sets the present mode to the vertical synchronous signal

1 extraction mode. Then, microcomputer 30 checks at step S432 whether the vertical synchronous  
2 signal V is input from horizontal/composite synchronous signal terminal HCS.

3 When the vertical synchronous signal V is input from horizontal/composite synchronous  
4 signal terminal HCS at the above step S432, microcomputer 30 determines at step S433 that the  
5 composite synchronous signal is input from horizontal/composite synchronous signal terminal HCS  
6 and the polarities of the vertical and horizontal synchronous signals V and H are both negative.  
7 Then, microcomputer 30 clamps the back porch of the horizontal synchronous signal H to the  
8 reference level of the picture to be displayed on CRT 60 and performs synchronous signal separation  
9 step S20.

10 However, when the vertical synchronous signal V is not input from horizontal/composite  
11 synchronous signal terminal HCS at the above step S432, microcomputer 30 determines at step S434  
12 that only the horizontal synchronous signal H is input from horizontal/composite synchronous signal  
13 terminal HCS. Then, microcomputer 30 clamps the front porch of the horizontal synchronous signal  
14 H to the reference level of the picture to be displayed on CRT 60 and performs synchronous signal  
15 separation step S20.

16 At the above step S520 of checking whether the composite synchronous signal or the  
17 separated vertical and horizontal synchronous signals V and H are input under the condition that the  
18 polarity of the horizontal synchronous signal H checked at step S510 is positive, as shown in Fig.  
19 5C, microcomputer 30 sets the polarity of the horizontal synchronous signal H to positive at step  
20 S521. Also, microcomputer 30 sets the present mode to the vertical synchronous signal extraction  
21 mode. Then, microcomputer 30 checks at step S522 whether the vertical synchronous signal V is  
22 input from horizontal/composite synchronous signal terminal HCS.

23 When the vertical synchronous signal V is input from horizontal/composite synchronous  
24 signal terminal HCS at the above step S522, microcomputer 30 determines at step S523 that the

1 composite synchronous signal is input from horizontal/composite synchronous signal terminal HCS  
2 and the polarities of the vertical and horizontal synchronous signals V and H are both positive.  
3 Then, microcomputer 30 clamps the back porch of the horizontal synchronous signal H to the  
4 reference level of the picture to be displayed on CRT 60 and performs synchronous signal separation  
5 step S20.

6 However, when the vertical synchronous signal V is not input from horizontal/composite  
7 synchronous signal terminal HCS at the above step S522, microcomputer 30 checks the polarity of  
8 the vertical synchronous signal V input from vertical synchronous signal terminal VS at step S524.

9 If the polarity of the vertical synchronous signal V checked at the above step S524 is  
10 positive, microcomputer 30 determines at step S525 that the separated vertical and horizontal  
11 synchronous signals V and H are input and the polarities thereof are both positive. Then,  
12 microcomputer 30 clamps the back porch of the horizontal synchronous signal H to the reference  
13 level of the picture to be displayed on CRT 60 and performs synchronous signal separation step S20.

14 When the polarity of the vertical synchronous signal V checked at the above step S524 is  
15 negative, microcomputer 30 determines at step S526 that the separated vertical and horizontal  
16 synchronous signals V and H are input, the polarity of the vertical synchronous signal V is negative  
17 and the polarity of the horizontal synchronous signal H is positive. Then, microcomputer 30 clamps  
18 the front porch of the horizontal synchronous signal H to the reference level of the picture to be  
19 displayed on CRT 60 and performs synchronous signal separation step S20.

20 At the above step S530 of checking whether the composite synchronous signal or the  
21 separated vertical and horizontal synchronous signals V and H are input under the condition that the  
22 polarity of the horizontal synchronous signal H checked at step S510 is negative, as shown in Fig.  
23 5D, microcomputer 30 sets the polarity of the horizontal synchronous signal H to negative at step  
24 S531. Also, microcomputer 30 sets the present mode to the vertical synchronous signal extraction

1 mode. Then, microcomputer 30 checks at step S532 whether the vertical synchronous signal V is  
2 input from horizontal/composite synchronous signal terminal HCS.

3 When the vertical synchronous signal V is input from horizontal/composite synchronous  
4 signal terminal HCS at the above step S532, microcomputer 30 determines at step S533 that the  
5 composite synchronous signal is input from horizontal/composite synchronous signal terminal HCS  
6 and the polarities of the vertical and horizontal synchronous signals V and H are both negative.  
7 Then, microcomputer 30 clamps the back porch of the horizontal synchronous signal H to the  
8 reference level of the picture to be displayed on CRT 60 and performs synchronous signal separation  
9 step S20.

10 However, when the vertical synchronous signal V is not input from horizontal/composite  
11 synchronous signal terminal HCS at the above step S532, microcomputer 30 checks the polarity of  
12 the vertical synchronous signal V input from vertical synchronous signal terminal VS at step S534.

13 If the polarity of the vertical synchronous signal V checked at the above step S534 is  
14 positive, microcomputer 30 determines at step S535 that the separated vertical and horizontal  
15 synchronous signals V and H are input, the polarity of the vertical synchronous signal V is positive  
16 and the polarity of the horizontal synchronous signal H is negative. Then, microcomputer 30 clamps  
17 the front porch of the horizontal synchronous signal H to the reference level of the picture to be  
18 displayed on CRT 60 and performs synchronous signal separation step S20.

19 When the polarity of the vertical synchronous signal V checked at the above step S534 is  
20 negative, microcomputer 30 determines at step S536 that the separated vertical and horizontal  
21 synchronous signals V and H are input and the polarities thereof are both negative. Then,  
22 microcomputer 30 clamps the front porch of the horizontal synchronous signal H to the reference  
23 level of the picture to be displayed on CRT 60 and performs synchronous signal separation step S20.



Fig. 6 is a block diagram illustrating the construction of microcomputer 30 in Fig. 3 for performing the synchronous signal separation operation in accordance with the present invention. As shown in this drawing, microcomputer 30 includes a multiplexer 75 for selecting one of the horizontal synchronous signal H or the composite synchronous signal from horizontal/composite synchronous signal terminal HCS and the synchronous-on-green signal from synchronous-on-green terminal SOG in response to a control signal C1, a vertical synchronous signal detector 71 for detecting the vertical synchronous signal V from an output signal from multiplexer 75, a multiplexer 76 for selecting the vertical synchronous signal V from vertical synchronous signal terminal VS or from vertical synchronous signal detector 71 in response to a control signal C2, a vertical synchronous signal polarity adjustment unit 72 for adjusting the polarity of the vertical synchronous signal V from multiplexer 76, a horizontal synchronous signal polarity adjustment unit 73 for adjusting the polarity of the horizontal synchronous signal H from multiplexer 76, a synchronous signal oscillator 74 for generating reference vertical and horizontal synchronous signals Vref and Href, a multiplexer 77 for selecting the vertical synchronous signal V from vertical synchronous signal polarity adjustment unit 72 or the reference vertical synchronous signal Vref from synchronous signal oscillator 74 in response to a control signal C3, and a multiplexer 78 for selecting the horizontal synchronous signal H from horizontal synchronous signal polarity adjustment unit 73 or the reference horizontal synchronous signal Href from synchronous signal oscillator 74 in response to control signal C3.

The synchronous signal separation operation of microcomputer 30 with the above-mentioned construction in accordance with the present invention will hereinafter be described in detail on the basis of the input forms of the vertical and horizontal synchronous signals V and H.

- 1) When separate vertical and horizontal synchronous signals V and H are input

1 In this case, the vertical synchronous signal V is input from vertical synchronous signal  
2 terminal VS and the horizontal synchronous signal H is input from horizontal/composite  
3 synchronous signal terminal HCS. Multiplexer 75 selects the horizontal synchronous signal H from  
4 horizontal/composite synchronous signal terminal HCS in response to control signal C1 and  
5 multiplexer 76 selects the vertical synchronous signal V from vertical synchronous signal terminal  
6 VS in response to control signal C2. Also, third and fourth multiplexers 77 and 78 select the output  
7 signals from vertical and horizontal synchronous signal polarity adjustment units 72 and 73 in  
8 response to control signal C3, respectively.

9 As a result, the vertical synchronous signal V from vertical synchronous signal terminal VS  
10 is selected by multiplexer 76, adjusted in polarity by vertical synchronous signal polarity adjustment  
11 unit 72 and then output through multiplexer 77. Also, the horizontal synchronous signal H from  
12 horizontal/composite synchronous signal terminal HCS is selected by multiplexer 75, adjusted in  
13 polarity by horizontal synchronous signal polarity adjustment unit 73 and then output through  
14 multiplexer 78.

15 2) When the composite synchronous signal is input

16 In this case, the composite synchronous signal is input from horizontal/composite  
17 synchronous signal terminal HCS. Multiplexer 75 selects the composite synchronous signal from  
18 horizontal/composite synchronous signal terminal HCS in response to control signal C1 and  
19 multiplexer 76 selects the output signal from vertical synchronous signal detector 71 in response to  
20 control signal C2. Also, multiplexers 77 and 78 select the output signals from vertical and horizontal  
21 synchronous signal polarity adjustment units 72 and 73 in response to control signal C3,  
22 respectively.

1 As a result, the composite synchronous signal from horizontal/composite synchronous signal  
2 terminal HCS is selected by multiplexer 75 and then applied to vertical synchronous signal detector  
3 71, which detects the vertical synchronous signal V from the composite synchronous signal.

4 Noticeably, vertical synchronous signal detector 71 can detect the vertical synchronous signal  
5 V from the composite synchronous signal in various manners. In the preferred embodiment of the  
6 present invention, vertical synchronous signal detector 71 utilizes a 5-bit counter to detect the  
7 vertical synchronous signal V from the composite synchronous signal, as will hereinafter be  
8 described in detail.

9 When multiplexer 75 selects the composite synchronous signal as shown in Fig. 7A from  
10 horizontal/composite synchronous signal terminal HCS, vertical synchronous signal detector 71 up-  
11 counts a clock signal (not shown) for a high level duration of the composite synchronous signal and  
12 down-counts the clock signal for a low level duration of the composite synchronous signal, as shown  
13 in Fig. 7B.

14 Vertical synchronous signal detector 71 generates a count within the range of "00000" to  
15 "11111". At this time, no underflow occurs when the count is below "00000" and no overflow  
16 occurs when the count is above "11111". Vertical synchronous signal detector 71 outputs a high  
17 level signal when the count is "11111".

18 In result, as shown in Fig. 7C, vertical synchronous signal detector 71 outputs a low level  
19 signal for a narrow pulse width interval of the horizontal synchronous signal H of the composite  
20 synchronous signal from multiplexer 75 because the count is below "11111" and a high level signal  
21 for a wide pulse width interval of the vertical synchronous signal V of the composite synchronous  
22 signal because the count is "11111".

1 The vertical synchronous signal V detected by vertical synchronous signal detector 71 is  
2 selected by multiplexer 76, adjusted in polarity by vertical synchronous signal polarity adjustment  
3 unit 72 and then output through multiplexer 77.

4 On the other hand, the composite synchronous signal from horizontal/composite synchronous  
5 signal terminal HCS is used directly as the horizontal synchronous signal H. As a result, the  
6 composite synchronous signal from horizontal/composite synchronous signal terminal HCS is  
7 selected by multiplexer 75, adjusted in polarity by horizontal synchronous signal polarity adjustment  
8 unit 73 and then output as the horizontal synchronous signal H through multiplexer 78.

9 3) When the synchronous-on-green signal is input

10 In this case, the synchronous-on-green signal is input from synchronous-on-green terminal  
11 SOG. Multiplexer 75 selects the synchronous-on-green signal from synchronous-on-green terminal  
12 SOG in response to control signal C1 and multiplexer 76 selects the output signal from vertical  
13 synchronous signal detector 71 in response to control signal C2. Also, multiplexers 77 and 78 select  
14 the output signals from vertical and horizontal synchronous signal polarity adjustment units 72 and  
15 73 in response to control signal C3, respectively.

16 As a result, the synchronous-on-green signal from synchronous-on-green terminal SOG is  
17 selected by multiplexer 75 and then applied to vertical synchronous signal detector 71, which detects  
18 the vertical synchronous signal V from the synchronous-on-green signal in a similar manner to the  
19 case where the composite synchronous signal is input.

20 The vertical synchronous signal V detected by vertical synchronous signal detector 71 is  
21 selected by multiplexer 76, adjusted in polarity by vertical synchronous signal polarity adjustment  
22 unit 72 and then output through multiplexer 77.

1 Also, the synchronous-on-green signal from synchronous-on-green terminal SOG is selected  
2 by multiplexer 75, adjusted in polarity by horizontal synchronous signal polarity adjustment unit 73  
3 and then output as the horizontal synchronous signal H through multiplexer 78.

4 4) When no Synchronous signal is input

5 In this case, microcomputer 30 outputs separate vertical and horizontal synchronous signals.  
6 In other words, synchronous signal oscillator 74 is operated, and multiplexers 77 and 78 select the  
7 output signals from synchronous signal oscillator 74 in response to control signal C3, respectively.

8 As a result, the reference vertical and horizontal synchronous signals Vref and Href from  
9 synchronous signal oscillator 74 are output through multiplexers 77 and 78, respectively.

10 As apparent from the above description, according to the present invention, the input forms  
11 of the vertical and horizontal synchronous signals from the computer system are discriminated in the  
12 software manner employing the microcomputer. In accordance with the discriminated input forms,  
13 the vertical and horizontal synchronous signals are separated from each other and then adjusted in  
14 polarity. Therefore, the present invention requires no separate hardware for the separation and  
15 polarity adjustment of the vertical and horizontal synchronous signals, resulting in simplification in  
16 circuit construction and reductions in number of used components and size of a printed circuit board.

17 Although the preferred embodiments of the present invention have been disclosed for  
18 illustrative purposes, those skilled in the art will appreciate that various modifications, additions and  
19 substitutions are possible, without departing from the scope and spirit of the invention as disclosed  
20 in the accompanying claims.

**WHAT IS CLAIMED IS:**

1           1.       A method for detecting and separating vertical and horizontal synchronous signals  
2 received by a monitor from a computer, comprising the steps of:

3               checking for inputs from a vertical synchronous signal terminal, a horizontal/composite  
4 synchronous signal terminal and a synchronous-on-green terminal of said computer to detect input  
5 forms of the vertical and horizontal synchronous signals from said computer; and

6               separating the vertical and horizontal synchronous signals from each other in accordance with  
7 the input forms detected during said step of checking and adjusting polarities of the separated  
8 vertical and horizontal synchronous signals.

1           2.       The method as set forth in Claim 1, wherein said step checking comprises the steps  
2 of:

3               checking said horizontal/composite synchronous signal terminal to determine whether the  
4 horizontal synchronous signal is input;

5               checking said vertical synchronous signal terminal to determine whether the vertical  
6 synchronous signal is input, when it is determined that the horizontal synchronous signal is not input  
7 from said horizontal/composite synchronous signal terminal;

8               checking said synchronous-on-green terminal to determine whether said horizontal  
9 synchronous signal is input, when it is determined that the vertical synchronous signal is not input  
10 from said vertical synchronous signal terminal; and

11              making a determination that no synchronous signal has been input and returning to said step  
12 of checking said horizontal/composite synchronous signal terminal, when it is determined that the  
13 horizontal synchronous signal is not input from said synchronous-on-green terminal.

1           3.     The method as set forth in claim 2, further comprising the steps of:  
2           checking said vertical synchronous signal terminal to determine whether the vertical  
3 synchronous signal is input, when it is determined that the horizontal synchronous signal is input  
4 from said horizontal/composite synchronous signal terminal;  
5           determining whether said horizontal synchronous signal has a positive polarity or a negative  
6 polarity, when it is determined that the horizontal synchronous signal is input from said  
7 horizontal/composite synchronous signal terminal and the vertical synchronous signal is not input  
8 from said vertical synchronous signal terminal;  
9           setting the polarity of said horizontal synchronous signal to positive and beginning a vertical  
10 synchronous signal extraction mode, when it is determined that said horizontal synchronous signal  
11 has a positive polarity;  
12           checking said horizontal/composite synchronous signal terminal to determine whether the  
13 vertical synchronous signal is input;  
14           making a determination that only the horizontal synchronous signal is input from said  
15 horizontal/composite synchronous signal terminal and performing a corresponding synchronous  
16 signal separation process, when it is determined that said vertical synchronous signal is not input  
17 from said horizontal/composite synchronous signal terminal; and  
18           making a determination that a composite synchronous signal is input from said  
19 horizontal/composite synchronous signal terminal, that the polarity of said horizontal and vertical  
20 synchronous signals are both positive and performing a corresponding synchronous signal separation  
21 process, when it is determined that said vertical synchronous signal is input from said  
22 horizontal/composite synchronous signal terminal.

1           4.     The method as set forth in claim 3, further comprising the steps of:  
2                 setting the polarity of said horizontal synchronous signal to negative and beginning a vertical  
3 synchronous signal extraction mode, when it is determined that said horizontal synchronous signal  
4 has a negative polarity;  
5                 checking said horizontal/composite synchronous signal terminal to determine whether the  
6 vertical synchronous signal is input;  
7                 making a determination that only the horizontal synchronous signal is input from said  
8 horizontal/composite synchronous signal terminal and performing a corresponding synchronous  
9 signal separation process, when it is determined that said vertical synchronous signal is not input  
10 from said horizontal/composite synchronous signal terminal; and  
11                 making a determination that a composite synchronous signal is input from said  
12 horizontal/composite synchronous signal terminal, that the polarity of said horizontal and vertical  
13 synchronous signals are both negative and performing a corresponding synchronous signal  
14 separation process, when it is determined that said vertical synchronous signal is input from said  
15 horizontal/composite synchronous signal terminal.

1           5.     The method as set forth in claim 3, further comprising the steps of:  
2                 determining whether said horizontal synchronous signal has a positive polarity or a negative  
3 polarity, when it is determined that the horizontal synchronous signal is input from said  
4 horizontal/composite synchronous signal terminal and the vertical synchronous signal is input from  
5 said vertical synchronous signal terminal;  
6                 setting the polarity of said horizontal synchronous signal to positive and beginning a vertical  
7 synchronous signal extraction mode, when it is determined that said horizontal synchronous signal  
8 has a positive polarity;



9 checking said horizontal/composite synchronous signal terminal to determine whether the  
10 vertical synchronous signal is input; and

11 making a determination that a composite synchronous signal is input from said  
12 horizontal/composite synchronous signal terminal, that the polarity of said horizontal and vertical  
13 synchronous signals are both positive and performing a corresponding synchronous signal separation  
14 process, when it is determined that said vertical synchronous signal is input from said  
15 horizontal/composite synchronous signal terminal.

1 6. The method as set forth in claim 5, further comprising the steps of:

2 determining whether said vertical synchronous signal from said vertical synchronous signal  
3 terminal has a positive polarity or a negative polarity, when it is determined that said vertical  
4 synchronous signal is not input from said horizontal/composite synchronous signal terminal;

5 making a determination that separate horizontal and vertical synchronous signals are input,  
6 that said horizontal and vertical synchronous signals have a positive polarity and performing a  
7 corresponding synchronous signal separation process, when it is determined that said vertical  
8 synchronous signal from said vertical synchronous signal terminal has a positive polarity; and

9 making a determination that separate horizontal and vertical synchronous signals are input,  
10 that said horizontal synchronous signal has a positive polarity, that said vertical synchronous signal  
11 has a negative polarity and performing a corresponding synchronous signal separation process, when  
12 it is determined that said vertical synchronous signal from said vertical synchronous signal terminal  
13 has a negative polarity.

1 7. The method as set forth in claim 5, further comprising the steps of:

2 setting the polarity of said horizontal synchronous signal to negative and beginning a vertical  
3 synchronous signal extraction mode, when it is determined that said horizontal synchronous signal  
4 has a negative polarity;

5 checking said horizontal/composite synchronous signal terminal to determine whether the  
6 vertical synchronous signal is input; and

7 making a determination that a composite synchronous signal is input from said  
8 horizontal/composite synchronous signal terminal, that the polarity of said horizontal and vertical  
9 synchronous signals are both negative and performing a corresponding synchronous signal  
10 separation process, when it is determined that said vertical synchronous signal is input from said  
11 horizontal/composite synchronous signal terminal.

1 8. The method as set forth in claim 7, further comprising the steps of:

2 determining whether said vertical synchronous signal from said vertical synchronous signal  
3 terminal has a positive polarity or a negative polarity, when it is determined that said vertical  
4 synchronous signal is not input from said horizontal/composite synchronous signal terminal;

5 making a determination that separate horizontal and vertical synchronous signals are input,  
6 that said horizontal synchronous signal has a negative polarity, that said vertical synchronous signals  
7 has a positive polarity and performing a corresponding synchronous signal separation process, when  
8 it is determined that said vertical synchronous signal from said vertical synchronous signal terminal  
9 has a positive polarity; and

10 making a determination that separate horizontal and vertical synchronous signals are input,  
11 that said horizontal and vertical synchronous signals have a negative polarity and performing a  
12 corresponding synchronous signal separation process, when it is determined that said vertical  
13 synchronous signal from said vertical synchronous signal terminal has a negative polarity.

1           9.     The method as set forth in claim 2, further comprising the steps of:  
2           making a determination that only the vertical synchronous signal has been input when it is  
3     determined that said vertical synchronous signal is input from said vertical synchronous signal  
4     terminal; and  
5           performing a corresponding synchronous signal separation process.

1           10.    The method as set forth in claim 2, further comprising the steps of:  
2           checking for input of said vertical synchronous signal from said synchronous-on-green  
3     terminal, when it is determined that said horizontal synchronous signal is input from said  
4     synchronous-on-green terminal;

5           making a determination that only the horizontal synchronous signal has been input from said  
6     synchronous-on-green terminal and performing a corresponding synchronous separation process,  
7     when it is determined that said vertical synchronous signal is not input from said synchronous-on-  
8     green terminal; and

9           making a determination that the vertical and horizontal synchronous signals are input from  
10    said synchronous-on-green terminal, setting the polarity of said vertical and horizontal synchronous  
11    signals to positive and performing a corresponding synchronous signal separation process, when it  
12    is determined that said vertical synchronous signal is input from said synchronous-on-green  
13    terminal.

1           11.    The method as set forth in claim 3, wherein said step of making a determination that  
2     only the horizontal synchronous signal is input from said horizontal/composite synchronous signal

terminal and performing a corresponding synchronous signal separation process further comprises a step of clamping a front porch of the horizontal synchronous signal to a reference level.

12. The method as set forth in claim 3, wherein said step of making a determination that a composite synchronous signal is input from said horizontal/composite synchronous signal terminal, that the polarity of said horizontal and vertical synchronous signals are both positive and performing a corresponding synchronous signal separation process further comprises a step of clamping a back porch of the horizontal synchronous signal to a reference level.

13. The method as set forth in claim 4, wherein said step of making a determination that only the horizontal synchronous signal is input from said horizontal/composite synchronous signal terminal and performing a corresponding synchronous signal separation process further comprises a step of clamping a front porch of the horizontal synchronous signal to a reference level.

14. The method as set forth in claim 4, wherein said step of making a determination that a composite synchronous signal is input from said horizontal/composite synchronous signal terminal, that the polarity of said horizontal and vertical synchronous signals are both negative and performing a corresponding synchronous signal separation process further comprises a step of clamping a back porch of the horizontal synchronous signal to a reference level.

15. The method as set forth in claim 5, wherein said step of making a determination that a composite synchronous signal is input from said horizontal/composite synchronous signal terminal, that the polarity of said horizontal and vertical synchronous signals are both positive and performing

4 a corresponding synchronous signal separation process further comprises a step of clamping a back  
5 porch of the horizontal synchronous signal to a reference level.

1 16. The method as set forth in claim 6, wherein said step of making a determination that  
2 separate horizontal and vertical synchronous signals are input, that said horizontal and vertical  
3 synchronous signals have a positive polarity and performing a corresponding synchronous signal  
4 separation process further comprises a step of clamping a back porch of the horizontal synchronous  
5 signal to a reference level.

1 17. The method as set forth in claim 6, wherein said step of making a determination that  
2 separate horizontal and vertical synchronous signals are input, that said horizontal synchronous  
3 signal has a positive polarity, that said vertical synchronous signal has a negative polarity and  
4 performing a corresponding synchronous signal separation process further comprises a step of  
5 clamping a front porch of the horizontal synchronous signal to a reference level.

1 18. The method as set forth in claim 7, wherein said step of making a determination that  
2 a composite synchronous signal is input from said horizontal/composite synchronous signal terminal,  
3 that the polarity of said horizontal and vertical synchronous signals are both negative and performing  
4 a corresponding synchronous signal separation process further comprises a step of clamping a back  
5 porch of the horizontal synchronous signal to a reference level.

1 19. The method as set forth in claim 8, wherein said step of making a determination that  
2 separate horizontal and vertical synchronous signals are input, that said horizontal synchronous  
3 signal has a negative polarity, that said vertical synchronous signals has a positive polarity and

4 performing a corresponding synchronous signal separation process further comprises a step of  
5 clamping a front porch of the horizontal synchronous signal to a reference level.

1 20. The method as set forth in claim 8, wherein said step of making a determination that  
2 separate horizontal and vertical synchronous signals are input, that said horizontal and vertical  
3 synchronous signals have a negative polarity and performing a corresponding synchronous signal  
4 separation process further comprises a step of clamping a front porch of the horizontal synchronous  
5 signal to a reference level.

1 21. The method as set forth in claim 1, further comprising a step of generating reference  
2 vertical and horizontal synchronous signals when no input is detected during said step of checking  
3 for inputs from said vertical synchronous signal terminal, said horizontal/composite synchronous  
4 signal terminal and said synchronous-on-green terminal of said computer.

1 22. The method as set forth in claim 2, wherein said step of making a determination that  
2 no synchronous signal has been input further comprises a step of generating reference vertical and  
3 horizontal synchronous signals.

1 23. A method for detecting and separating vertical and horizontal synchronous signals  
2 received by a monitor from a computer, comprising the steps of:

3 checking for inputs from a vertical synchronous signal terminal, a horizontal/composite  
4 synchronous signal terminal and a synchronous-on-green terminal of said computer to detect input  
5 forms of the vertical and horizontal synchronous signals from said computer;



**ABSTRACT OF THE DISCLOSURE**

A method for detecting and separating vertical and horizontal synchronous signals from a computer system. The input forms of the vertical and horizontal synchronous signals from the computer system are detected by scanning a vertical synchronous signal terminal, a horizontal/composite synchronous signal terminal and a synchronous-on-green terminal of the computer system. In accordance with the detected input forms, the vertical and horizontal synchronous signals are separated from each other and then adjusted in polarity. Therefore, the present invention requires no separate hardware for the separation and polarity adjustment of the vertical and horizontal synchronous signals, resulting in simplification in circuit construction and reductions in number of used components and size of a printed circuit board.



FIG. 1

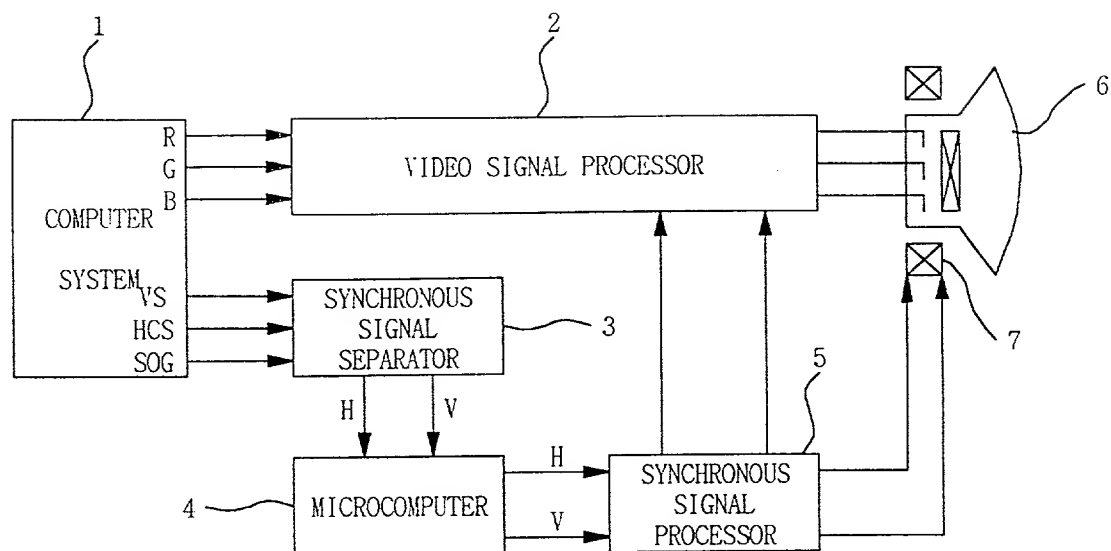


FIG. 2A

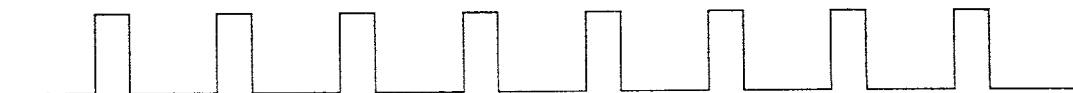


FIG. 2B

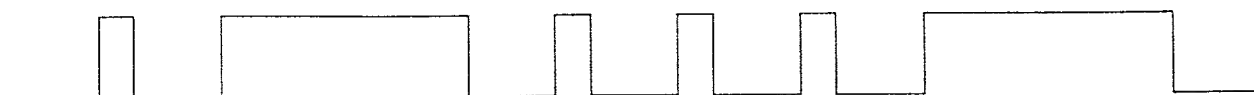


FIG. 2C

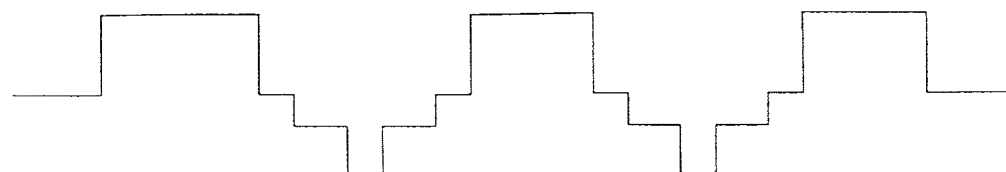


FIG. 3

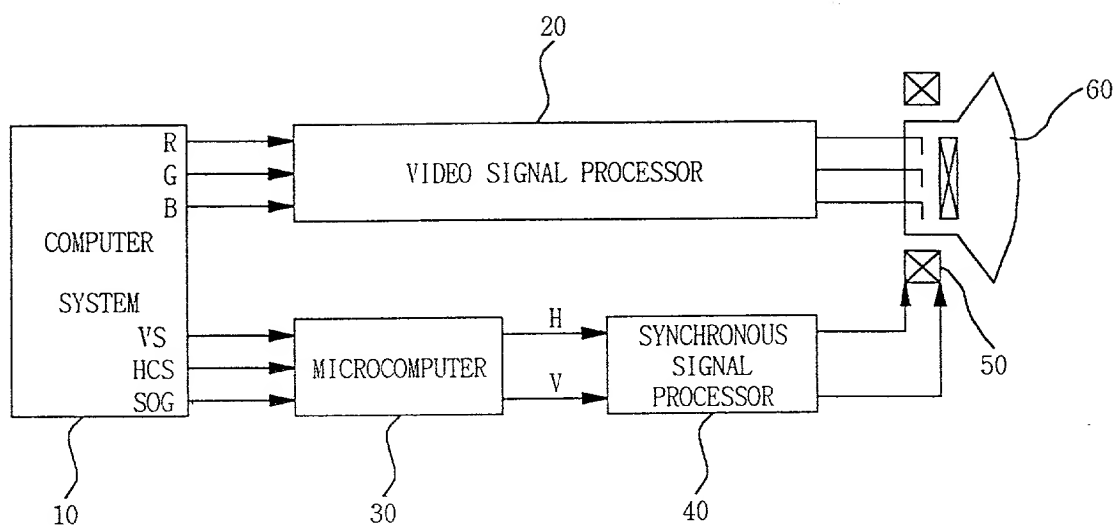


FIG. 4

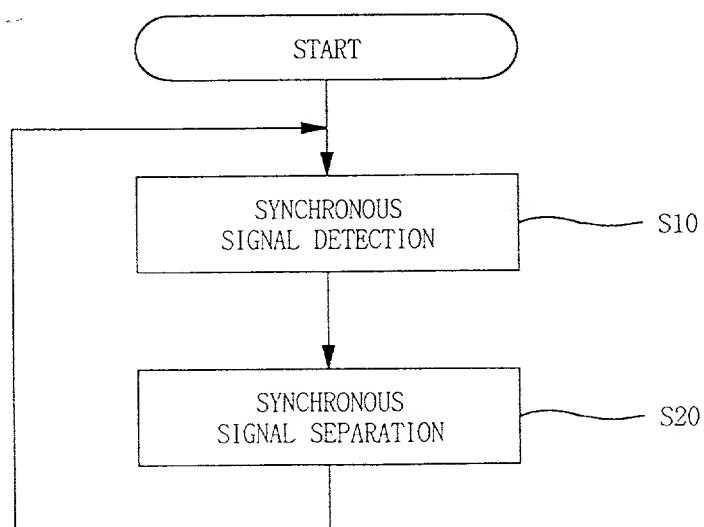


FIG. 5A

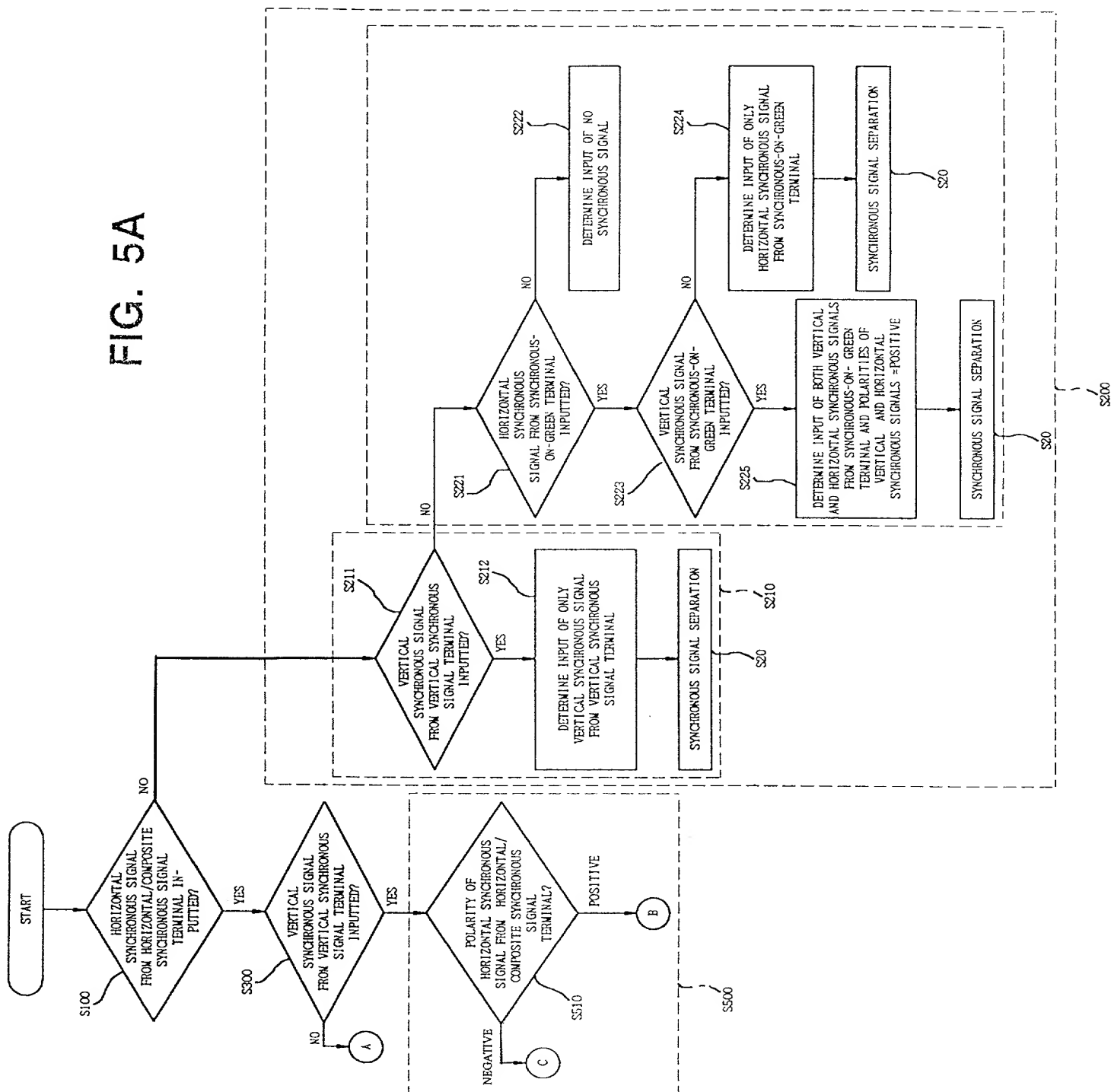
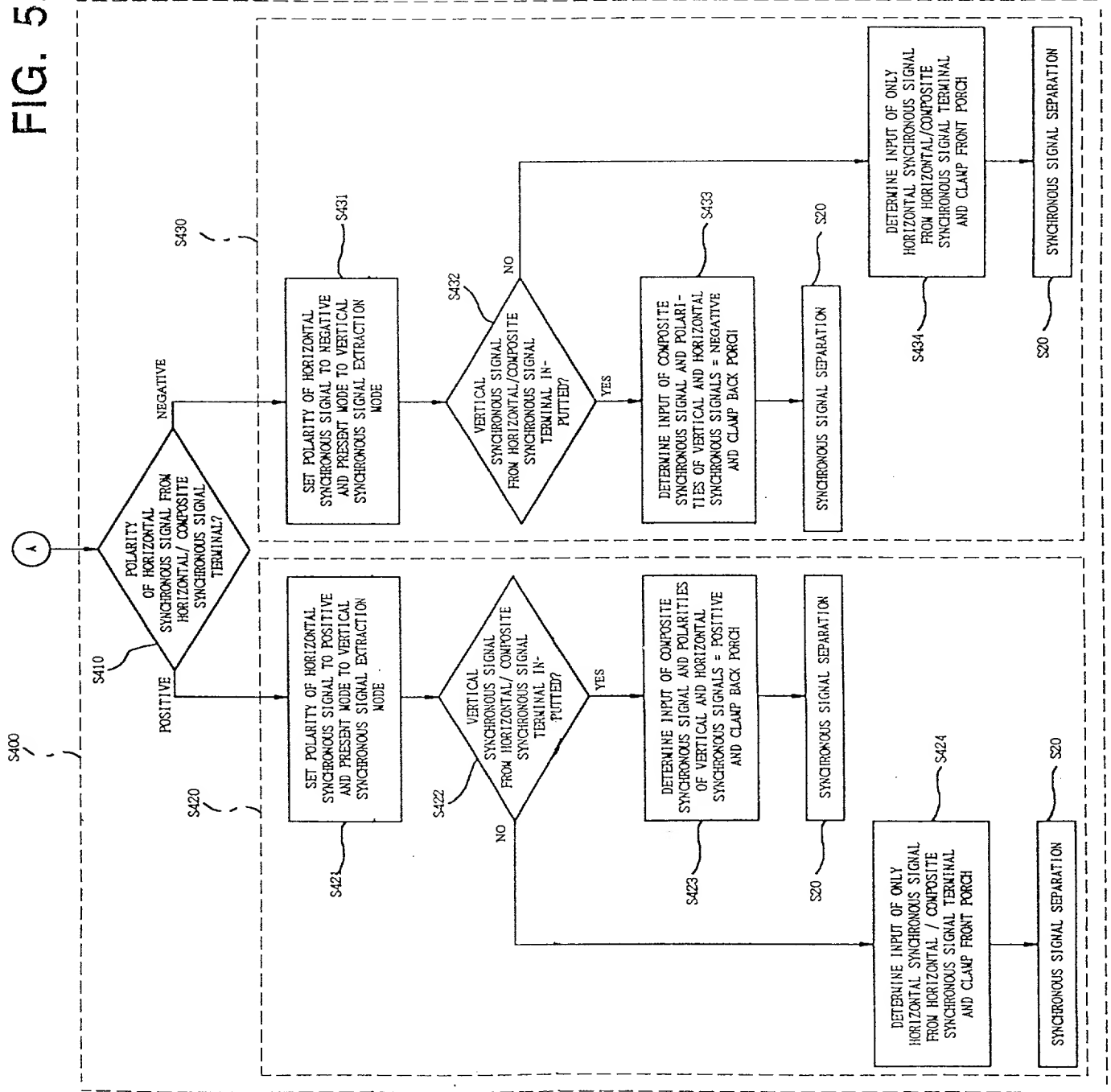


FIG. 5B



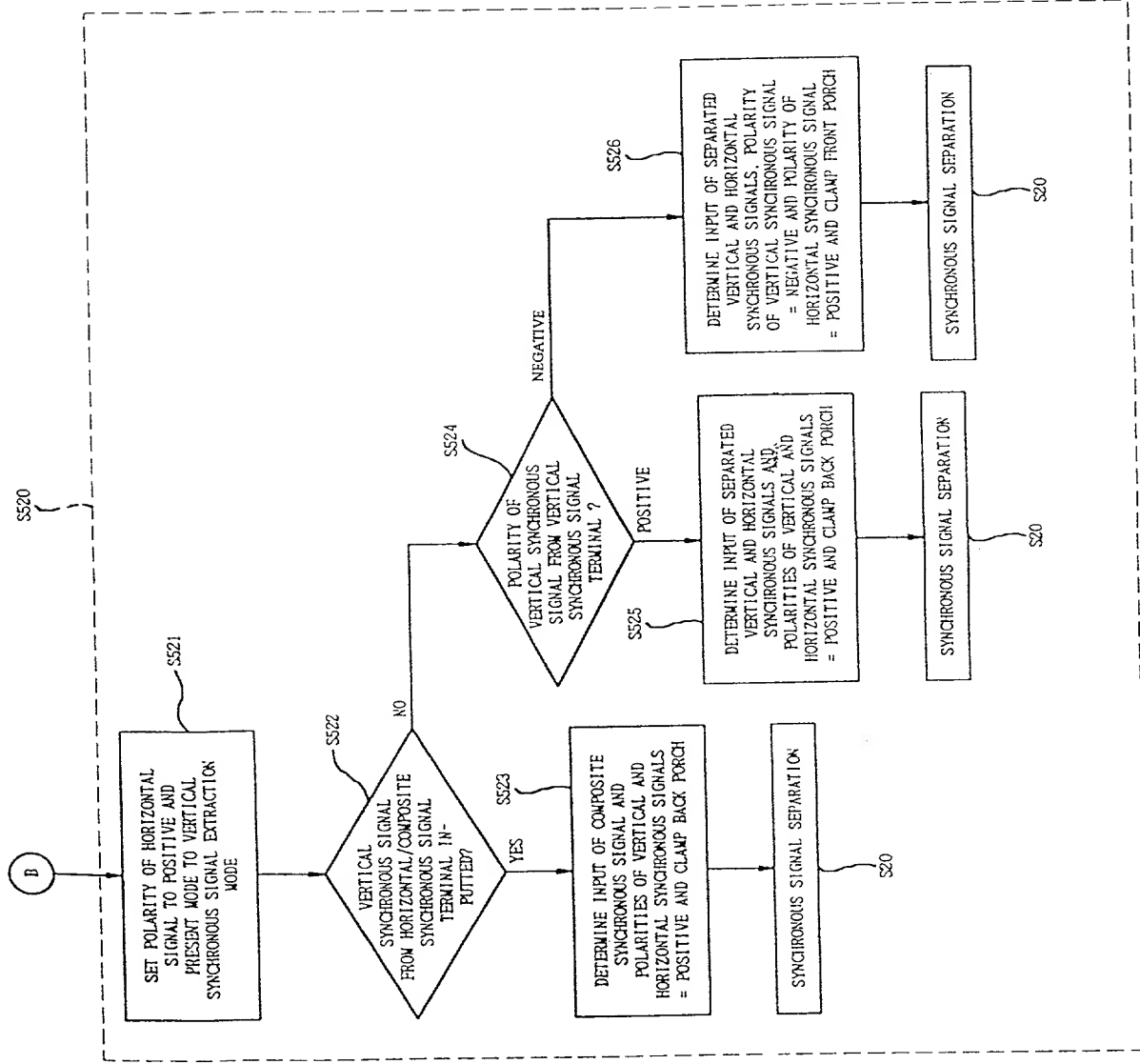


FIG. 5C

FIG. 5D

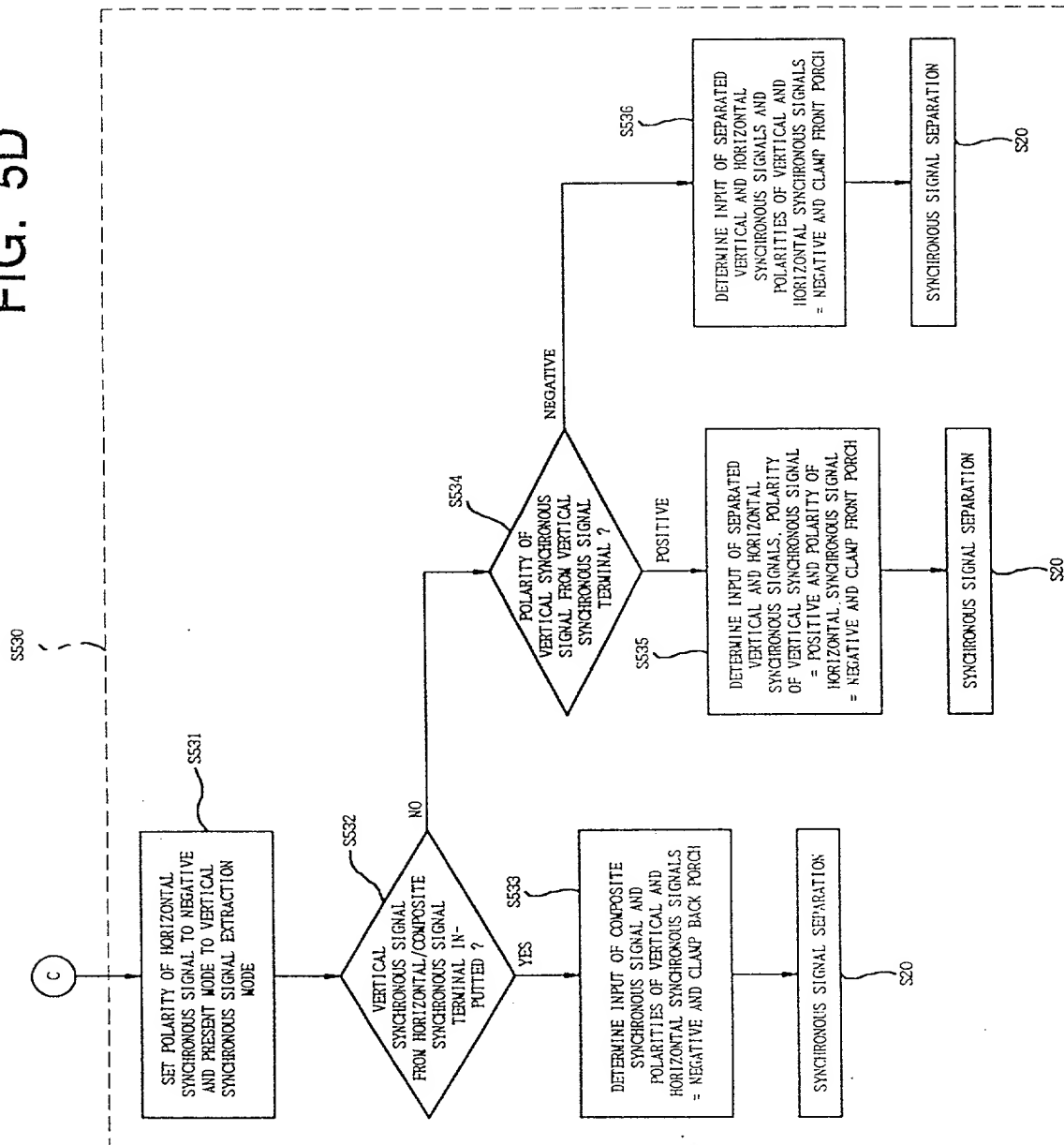


FIG. 6

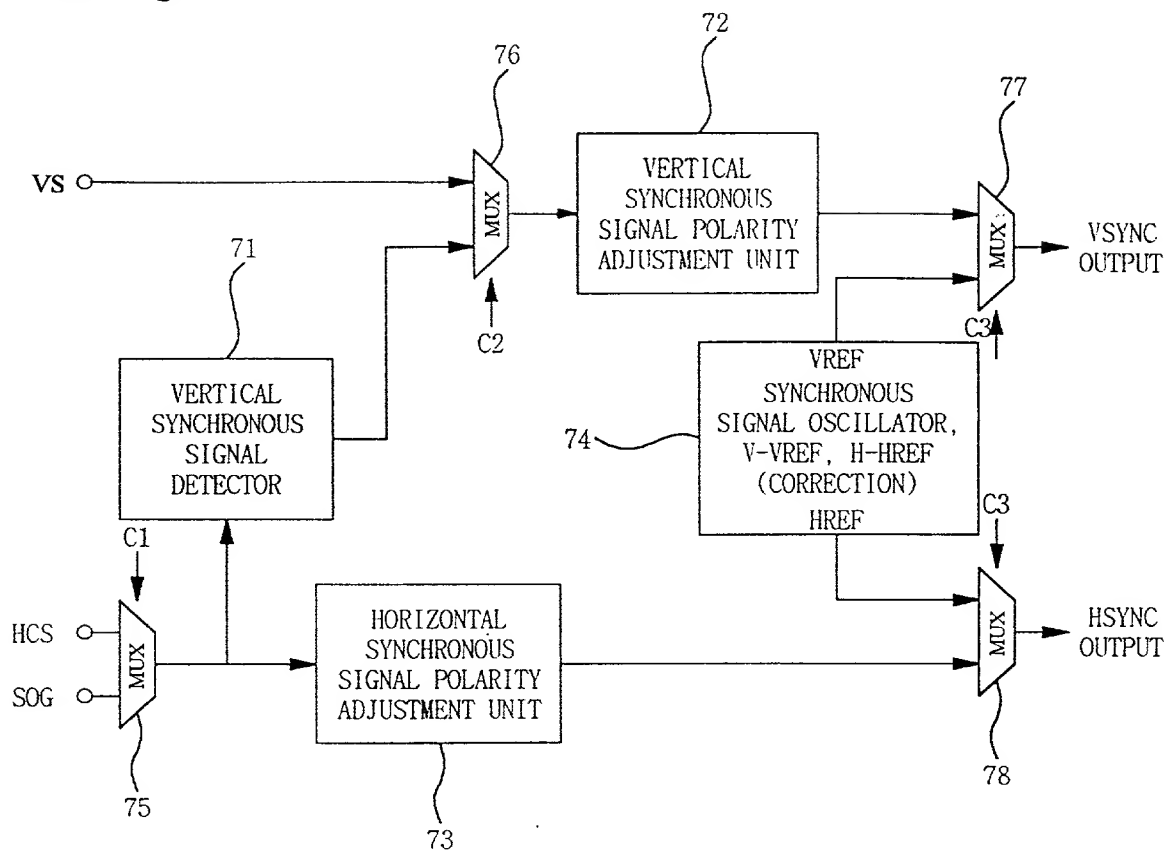


FIG. 7A

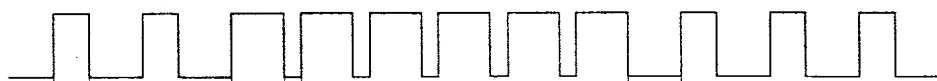
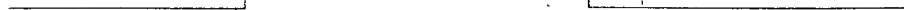


FIG. 7B



FIG. 7C



## DECLARATION

AS A BELOW NAMED INVENTOR, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole (if only one name is listed below), or an original, first and joint inventor (if plural names are listed below), of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**TITLE:** METHOD FOR DETECTING AND SEPARATING VERTICAL AND HORIZONTAL  
SYNCHRONOUS SIGNALS FROM COMPUTER SYSTEM

the specification of which either is attached hereto or otherwise accompanies this Declaration, or:

☐ was filed in the U.S. Patent & Trademark Office on \_\_\_\_\_ and assigned Serial No. \_\_\_\_\_,

☐ and (if applicable) was amended on \_\_\_\_\_

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability and to the examination of this application in accordance with Title 37 of the Code of Federal Regulations §1.56. I hereby claim foreign priority benefits under Title 35, U.S. Code §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, or §119(e) of any United States provisional application(s), listed below and have also identified below any foreign applications for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

P96-22949      Rep. of Korea      21/06/1996  
(Application Number)      (Country)      (Day/Month/Year filed)

Priority Claimed:  
Yes [ X ] No [ ]

\_\_\_\_\_  
(Application Number)      (Country)      (Day/Month/Year filed)

Yes [ ] No [ ]

\_\_\_\_\_  
(Application Number)      (Country)      (Day/Month/Year filed)

Yes [ ] No [ ]

I hereby claim the benefit under Title 35, U.S. Code, §120, of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of Title 35, U.S. Code, §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, The Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

\_\_\_\_\_  
(Application Serial No.)      (Filing Date)      (STATUS: patented, pending, abandoned)

\_\_\_\_\_  
(Application Serial No.)      (Filing Date)      (STATUS: patented, pending, abandoned)

I hereby appoint the following attorneys: Robert E. Bushnell, Reg. No. 27,774, and Michael D. Parker, Reg. No. 34,973, to prosecute this application and to transact all business in the U.S. Patent & Trademark Office connected therewith and with any divisional, continuation, continuation-in-part, reissue or re-examination application, with full power of appointment and with full power to substitute an associate attorney or agent, and to receive all patents which may issue thereon, and request that all correspondence be addressed to:

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I HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 U.S. Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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FULL NAME OF SECOND JOINT INVENTOR: \_\_\_\_\_

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Date: \_\_\_\_\_

FULL NAME OF THIRD JOINT INVENTOR: \_\_\_\_\_

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FULL NAME OF FOURTH JOINT INVENTOR: \_\_\_\_\_

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☐ Additional inventors are being named on separately numbered sheets attached hereto.